CLAIMS

What is claimed is:

1. An integrated digital subscriber line transceiver, comprising:

a single integrated circuit having:

a digital signal processing engine adapted to couple the transceiver to at least one digital subscriber line communication link;

a time division multiplexing framer adapted to couple the transceiver to at least one time division multiplexing communication link;

a static random access memory; and

a microprocessor coupled to the digital signal processing engine, the time division multiplexing framer, and the static random access memory.

2. The integrated transceiver of claim 1, wherein the digital signal processing engine is adapted to couple the transceiver to the digital subscriber line communication link using an analog front end.

3. The integrated transceiver of claim 1, wherein the time division multiplexing framer is adapted to couple the transceiver to one time division multiplexing communication link using a time division multiplexing line interface unit.

4. The integrated transceiver of claim 1, wherein the single integrated circuit further includes a bus coupled to the digital signal processing engine, the time division multiplexing framer, the microprocessor and the static random access memory.

5. The integrated transceiver of claim 1, wherein the digital signal processing engine includes a digital subscriber line data pump adapted to couple the digital signal processing engine to the at least one digital subscriber line communication link.

6. The integrated transceiver of claim 5, wherein the digital signal processing engine includes a digital subscriber line framer coupled to the digital subscriber line data pump and the time division multiplexing framer.

7. The integrated transceiver of claim 1, wherein the digital signal processing engine includes an HDSL2 digital signal processing engine.

8. The integrated transceiver of claim 1, wherein the digital signal processing engine includes a G.SHDSL digital signal processing engine.

9. The integrated transceiver of claim 1, wherein the time division multiplexing framer includes a T1/E1 framer.

10. A digital subscriber line unit, comprising:

an analog interface adapted to couple the digital subscriber line unit to at least one digital subscriber line communication link;

a time division multiplexing line interface unit adapted to couple the digital subscriber line unit to at least one time division multiplexing communication link; and

an integrated digital subscriber line transceiver, comprising:

a single integrated circuit having:

a digital signal processing engine coupled to the analog interface;

a time division multiplexing framer coupled to the time division multiplexing line interface unit;

a static random access memory; and

a microprocessor coupled to the digital signal processing engine, the time division multiplexing framer, and the static random access memory.

11. The digital subscriber line unit of claim 10, wherein the single integrated circuit further includes a bus coupled to the digital signal processing engine, the time division multiplexing framer, the microprocessor and the static random access memory.

12. The digital subscriber line unit of claim 10, wherein the digital signal processing engine includes a digital subscriber line data pump adapted to couple the digital signal processing engine to the analog front end.

13. The digital subscriber line unit of claim 12, wherein the digital signal processing engine includes a digital subscriber line framer coupled to the digital subscriber line data pump and the time division multiplexing framer.

14. The digital subscriber line unit of claim 10, wherein the digital signal processing engine includes an HDSL2 digital signal processing engine.

15. The digital subscriber line unit of claim 10, wherein the digital signal processing engine includes a G.SHDSL digital signal processing engine.

16. The digital subscriber line unit of claim 10, wherein the time division multiplexing framer includes a T1/E1 framer.

17. The digital subscriber line unit of claim 10, wherein the analog interface includes:

a hybrid circuit adapted to couple the analog interface to the at least one digital subscriber line communication link;

a line driver coupled to the hybrid circuit; and

an analog front end coupled to the line driver and the integrated transceiver.

18. The digital subscriber line unit of claim 10, wherein the time division multiplexing line interface unit includes a T1/E1 line interface unit.

19. An integrated digital subscriber line transceiver, comprising:

a single integrated circuit having:

a digital signal processing engine adapted to couple the transceiver to at least one digital subscriber line communication link and to at least one time division multiplexing communication link;

a static random access memory; and

a microprocessor coupled to the digital signal processing engine and the static random access memory.

20. The integrated transceiver of claim 20, wherein the digital signal processing engine is adapted to couple the transceiver to at least one digital subscriber line communication link using an analog front end and to at least one time division multiplexing communication link using a time division multiplexing line interface unit.

21. The integrated transceiver of claim 20, wherein the single integrated circuit further includes a bus coupled to the digital signal processing engine, the microprocessor and the static random access memory.

22. The integrated transceiver of claim 20, wherein the digital signal processing engine includes a digital subscriber line data pump adapted to couple the digital signal processing engine to the at least one digital subscribe line communication link.

23. The integrated transceiver of claim 22, wherein the digital signal processing engine includes a digital subscriber line framer coupled to the digital subscriber line data pump.

24. The integrated transceiver of claim 20, wherein the digital signal processing engine includes an HDSL2 digital signal processing engine.

25. The integrated transceiver of claim 20, wherein the digital signal processing engine includes a G.SHDSL digital signal processing engine.

26. A digital subscriber line unit, comprising:

an analog interface adapted to couple the digital subscriber line unit to at least one digital subscriber line communication link;

a time division multiplexing line interface unit adapted to couple the digital subscriber line unit to at least one time division multiplexing communication link; and

a time division multiplexing framer coupled to the time division multiplexing line interface unit;

an integrated digital subscriber line transceiver, comprising:

a single integrated circuit having:

a digital signal processing engine coupled to the analog interface and the time division multiplexing framer;

a static random access memory; and

a microprocessor coupled to the digital signal processing engine, the time division multiplexing framer, and the static random access memory.

27. The digital subscriber line unit of claim 26, wherein the digital signal processing engine includes a digital subscriber line data pump adapted to couple the digital signal processing engine to the at least one digital subscriber line communication link.

28. The digital subscriber line unit of claim 27, wherein the digital signal processing engine includes a digital subscriber line framer coupled to the digital subscriber line data pump and the time division multiplexing framer.

29. The digital subscriber line unit of claim 26, wherein the digital signal processing engine includes an HDSL2 digital signal processing engine.

30. The digital subscriber line unit of claim 26, wherein the digital signal processing engine includes a G.SHDSL digital signal processing engine.

31. The digital subscriber line unit of claim 26, wherein the time division multiplexing framer includes a T1/E1 framer.

32. The digital subscriber line unit of claim 26, wherein the analog interface includes:

a hybrid circuit adapted to couple the analog interface to the at least one digital subscriber line communication link.

a line driver coupled to the hybrid circuit; and

an analog front end coupled to the line driver and the integrated transceiver.

33. The digital subscriber line unit of claim 26, wherein the time division multiplexing line interface unit includes a T1/E1 line interface unit.

34. The digital subscriber line unit of claim 26, wherein the time division multiplexing framer unit includes a T1/E1 framer.